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Nearly Exact Signal Probabilities for Synchronous Sequential Circuits – an Experimental Analysis

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Abstract

In this article we present a strategy how to estimate the signal probabilities for synchronous sequential circuits. For each line in the circuit an OBDDs is constructed only once. Using this OBDD the signal probabilities in every succeeding time frame is computed. We investigated a large set of the ISCAS'89 benchmark circuits, showing that the proposed strategy estimates 75% *of all signals considered with a relative error of only* 10% *or less.*

1. Extended Introduction

The knowledge of signal probabilities and fault detection probabilities has been proven useful almost everywhere in the area of deterministic and random testing of combinational circuits. This knowledge is even more valuable for sequential circuits. For combinational circuits, highly efficient tools have been developed for that task. Some base on sophisticated approximation strategies [8, 11, 17], other compute the exact value [7, 10, 12]. An other important application of signal probabilities is switching activity analysis as shown e.g. in [16]. Even in the case of a combinational circuit, the exact algorithms have exponential time complexity measured in the number of inputs. So, we do not expect an efficient exact algorithm for all synchronous sequential circuits, but heuristics approximating the real value.

Here, we consider an iterative network representation of the finite state machine, using the gate level realization. For that, we assume *secondary inputs* and *secondary outputs* representing the outputs and inputs of the memory elements. We compute an estimation of the signal probabilities of every lead (signal) in the circuit over a given number of time frames similar to a Markov-process. For this work, we also compute the real signal probabilities by symbolic methods, as far as possible. Thus, we can show the accuracy of the estimation by computing the relative error for each lead. To our knowledge, in literature no work has been presented, considering an estimation of the signal probability for each line in a sequential circuit over the progress of time. Only some related work has been presented, that base on considering the sequential circuit as a Markov-chain, especially in the area of verification. For example with reachability analysis probabilistic approaches [2, 3, 4, 5, 6, 14] outreach symbolic approaches, e.g. [9, 15]. Other related work focus on the probability of the existence of a random reset sequence [13].

1.1. Exact Signal Probability

The signal probability of a line in the circuit denotes the chance, that this particular line assumes the boolean value *one*. Given on OBDD [1] this value can efficiently be determined:

- With $P_r(x_i = 1)$, $P_r(x_i = 0)$ we denote the probability that a boolean variable x_i assumes the value one or zero, respectively. $P_r(g = 1)$ for a boolean function g gives the probability that g assumes the value one for a random argument.
- Let $G = (V, E)$ be an OBDD with set of nodes V and set of edges E. Each node in V is labeled with a boolean variable out of $\{x_1, \ldots, x_n\}$. Let $u \in V$ be the root node of G, and let G represent the function $g_u : \mathbb{B}^n \to \mathbb{B}$.
- The probability $P_r(g_u = 1)$ can be computed in time $O(|G|)$ using the recursive function $P : V \to [0, 1] \subset \mathbb{R}$ with $P(v) = 1$ ($P(v) = 0$) if v is the terminal one node (terminal zero node) and
$$P(v) = P_r(x(v) = 0) \cdot P(w_l) + P_r(x(v) = 1) \cdot P(w_h) \tag{1}$$
otherwise, where $x(v)$ is the boolean variable, assigned to node v and w_l and w_h are the *low* and the *high* sons of v, respectively.

We identify the signal probability $P_r(l = 1)$ of a lead (signal) l in the circuit with $P_r(g_u = 1)$ of the according function at this lead. Thus, with combinational circuits the exact signal probabilities can be computed by:

1. Constructing an OBDD for every lead of the circuit.
2. Evaluating the OBDDs with Formula 1 shown above.

With a straightforward approach the exact signal probabilities for a synchronous sequential circuit can be determined as shown below. For sure, this approach cannot handle many time frames, but it is sufficient for our purpose. It constructs the OBDDs of every lead in the circuit by substitution and evaluates the signal probabilities, before it continues with the next time frame:

1. For the first time frame:
   (a) Construct the OBDD for every lead of the circuit.
   (b) Evaluate the OBDDs with Formula 1 shown above.
   (c) Store all OBDDs.
2. For every next time frame:
   (a) Construct new functions by substituting the boolean variables formerly assigned to the primary inputs by a new set of variables, representing the primary inputs of the new time frame. Do this for all stored OBDDs.

(b) Substitute in all OBDDs constructed in the step before the boolean variables, formerly assigned to the secondary inputs by the function at the input lead of the according memory element of the time frame before.

(c) Evaluate the OBDDs with Formula 1 shown above.

1.2. Signal Probability Estimation

The problem of the algorithm above, and other algorithms doing symbolic state space traversal, is the space and time complexity. Some research considering other types of decision diagrams has been done. Probabilistic approximations are also an alternative to handle the complexity. With our strategy, we make exact computations within each time frame. We only loose the precision between the time frames, by not regarding the dependencies of the memory elements. Thus, we consider each memory element as *independent*. W.o.l.g. let $\{x_1, \ldots, x_m\}$ be the variables assigned to the secondary inputs before the first time frame, and let f_i, $1 \leq i \leq m$, be the functions at the input leads of the secondary outputs of the first time frame. The strategy is as follows:

1. For the first time frame:

   (a) Construct the OBDD for every lead of the circuit.

   (b) Evaluate the OBDDs with Formula 1 shown above.

2. For every next time frame:

   (a) Modify the probability of $\{x_1, \ldots, x_m\}$ by:

   $$P_r(x_i = 0) := 1 - P_r(f_i = 1), \quad P_r(x_i = 1) := P_r(f_i = 1), \quad 1 \leq i \leq m$$

   (b) Evaluate the OBDDs with Formula 1 shown above.

With this strategy, we pursue the following: Compute the signal probabilities as accurate as possible by evaluating the OBDD. At every next time frame, compute the signal probabilities of the current time frame by assuming the signal probabilities for the secondary inputs, defined by the signal probability of the input lead of the according secondary output one time frame before. Thus, we consider the signal correlation within a time frame, but not over the time frame boundary. Note, that we do not have different sets of primary input variables for every time frame. This is implicitly 'given' by the modified signal probability of the secondary inputs.
Of course, the values computed by this strategy have an inherent error. Let P_r^{real} (P_r^{est}) represent the real (estimated) signal probability. We compute the *relative error (RE)* at lead l by:

$$RE(l) = \left| \frac{P_r^{real}(l = 1) - P_r^{est}(l = 1)}{P_r^{real}(l = 1)} \right|$$

Thus, $RE(l)$ gives the percentage with that the estimated value P^{est} differs from the real value P^{real}. In the next section our experimental results show, that for most circuits the approximation is very accurate.

Circuit	#TF	#Sig.	Total	0%	0%-5%	5%-10%	10%-20%	20%-30%	30%-50%	> 50%
s00027	14	17	238	116	82			40		
s00208.1	14	122	1708	1708						
s00298	10	136	1360	331	422	69	160	27	89	262
s00344	4	184	736	200	222	100	51	57	50	56
s00349	4	185	740	204	222	100	51	57	50	56
s00382	6	182	1092	231	414	80	72	49	54	192
s00386	6	172	1032	108	362	111	91	54	87	219
s00400	6	186	1116	232	437	80	72	49	54	192
s00420	14	252	3528	3528						
s00444	5	205	1025	196	454	76	66	32	54	147
s499	14	175	2450	71	1051	69	91	66	128	974
s00510	4	236	944	146	430	129	141	45	37	16
s00526n	4	218	872	176	313	83	60	19	52	169
s635	9	320	2880	346	1696	12	13	8	28	777
s00641	1	433	433	218	141	20	37		6	11
s00713	1	447	447	234	136	20	37		6	14
s00820	2	312	624	167	237	54	60	19	12	75
s00832	3	310	930	205	405	74	82	28	27	109
s938	4	512	2048	2048						
s00953	2	440	880	212	308	37	33	18	66	206
s01196	6	561	3366	2936	369	19	12	17	13	
s01238	4	540	2160	1880	231	21	8	11	9	
s01494	4	661	2644	148	252	218	297	241	325	1163
Sum			33253	15641	8184	1302	1434	837	1147	4638
				47.04%	24.61%	3.92%	4.31%	2.52%	3.45%	13.95%
				25127, 75.56%					5785, 17.40%	
				26561, 79.88%						

Table 1. Distribution of the relative error.

2. Experimental Results

For our first measurements (Table 1), we selected all small ISCAS'89 benchmark circuits (first column) for that we can built up the OBDDs for several succeeding time frames. Initially $P_r(x_i = 1)$ is set to 0.5 for all i. The execution times are determined by the iterated OBDD construction. Once having the OBDDs for the first time frame only, computing the estimated signal probabilities is a matter of seconds, even for a large number of time frames. Due to the computation complexity of the OBDD-part we have to limit the number of time frames considered. Column two gives the number of time frames for that we computed an estimation and the relative error. The minimum is given for circuit $s00641$ and for circuit $s00713$. The maximum was set to 14. (This means, the estimation is done for the time frames 2 to 15.) The third column gives the number of signals of the circuit. The next column shows the total number of signals considered. This is the number of time frames times the number of signals of the circuit. The next seven columns show the distribution of the relative error. The first column gives the number of signals, for that the estimated signal probabilities match exactly the computed ones. The next column shows the number of signals,

Circuit	TF	0%	0%-5%	5%-10%	10%-20%	20%-30%	30%-50%	$> 50\%$
s00298	2	70	19	13	8	6	11	8
	3	29	36	16	12	7	11	25
	4	29	37	10	21	2	5	37
	5	29	39	7	22		9	30
	6	29	42	7	19	2	10	27
	7	29	48	4	17	3	5	31
	8	29	48	4	15	1	11	28
	9	29	49	3	17		9	29
	10	29	51	2	14	2	11	24
	11	29	53	3	15	4	7	25
s01196	2	496	54	4	2	2	3	
	3	488	63	3	2	3	2	
	4	488	63	3	2	3	2	
	5	488	63	3	2	3	2	
	6	488	63	3	2	3	2	
	7	488	63	3	2	3	2	
s01494	2	67	68	58	70	60	93	245
	3	27	70	54	76	66	85	283
	4	27	66	53	75	54	85	301
	5	27	48	53	76	61	62	334

Table 2. Distribution of the relative error over the time frames.

for that the error ranges in the interval $(0\%, 5\%]$. The following columns are accordingly. Note, that in the last column some entries result from division by zero. More in detail: If the real value is zero but the estimated is not, the relative error is ∞, although the estimation is very small (less than 1% signal probability). Also note, that there are a number of values of magnitude 10^{-10} and smaller. These may occur due to rounding errors. However, these values are treated as non-zero values. For most lines that have a large relative error we notice, that the real signal probability is small (less than 5%) or even smaller (mostly less than 1%), but the the strategy overestimated the value in most cases. A typical result is a real value of 0.5% signal probability and an estimation of 1%, resulting in a relative error of 50%. However, both values have the same magnitude.

Summing up these results, we can state, that more than 47% of the signal probabilities are computed *exactly*, and for another 24% we have an relative error of only 5% at maximum. On the other hand for only 14% the error is larger than 50%. Widening the considered range, only 17% of the signal probabilities have an error larger than 30%, whereas more than 75% have an error less or equal to 10%. Finally, nearly 80% of all signal probabilities are estimated with a relative error of less or equal to 20%.

Table 2 shows the progress of the relative error from time frame to time frame. We selected three circuits shown in more detail. One circuit with bad results ($s01494$), one with very good results ($s01196$), and one intermediate ($s00298$). Here TF gives the number of the time frame.

For circuit $s00298$ we can see, that it starts with a wide distribution of relative errors. As the algorithm continues, the distribution varies only slightly. The same holds even stronger for $s01196$.

Circuit	TF	Circuit	TF
s00027	-	s00510	-
s00208.1	3	s00526n	-
s00298	-	s635	778
s00344	-	s00641	-
s00349	-	s00713	-
s00382	238	s00820	43
s00386	38	s00832	43
s00400	238	s948	3
s00420	3	s00953	187
s00444	141	s01196	5
s499	45	s01238	5
		s01494	29

Table 3. Stabilization of the estimation.

Additionally, beginning with time frame four, the relative errors of the signals remain the same. The same conclusion can be drawn for circuit $s01494$.
From these observations, we conclude, that we can see after a few time frames, if our estimation is accurate or not. However, some few circuits seem to attract the relative errors to both ends of the distribution. It is not clear up to now, if this is tied to the fact considered in the next table.
As in other probabilistic approaches, our strategy considers the sequential circuit similar to a Markov-chain. Under special circumstances such processes have the property to stabilize. That is, the current values do not differ from the values before. In our experiments this means the estimated probabilities of each line in the circuit at the actual time frame and the time frame before are identical. Results can be found in Table 3. We had an upper limit of 1000 time frames. If an estimation did not stabilize until then, it is shown here by a '–' sign.

3. Conclusions and Future Work

In this work we considered the problem of computing signal probabilities for synchronous sequential circuits. We combined the exact evaluation within each time frame using OBDDs with a probabilistic approach transferring the information from one time frame to the next. With our method, we regard signal correlations within each time frame, but disregard them over the time frame boundaries. Thus, our estimation for the real signal probabilities has an inherent error. We showed by a large set of experiments, that this error is usually very small. In fact, more than 3/4 of all values are approximated with an error less or equal to 10%. On the other hand side, we need not construct the OBDDs for each time frame, but the first. For the circuits considered, this can be done efficiently using any OBDD package available.
For future work, we try to identify properties of those leads of the circuit with a worse estimation. From this information we hope to derive conclusions, that help to estimate the relative error a priory, without constructing the OBDD for several time frames.
Finally, we will extend the method presented to compute an estimation of the fault detection probabilities for sequential circuits.

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